REMARKS

Applicant has reviewed and considered the office action mailed on May 15, 2003 and the references cited therewith.

Claim 4 is amended, and claims 29-37 are added; as a result, claims 4-6, 9-10, 14-16, and 29-37 are pending in the above-referenced patent application.

The amendment to claim 4 finds support, for example, at page 6, lines 9 and 10 of the specification. New claims 29-37 find support, for example, at page 6, lines 1-20 of the specification.

Claim Objections

Claims 4-6 and 14-16 were objected to due to informalities. Applicant respectfully traverses the objection to claim 14.

Claim 4, as amended, does not include the language that was the focus of the objection. Claims 5 and 6 are dependent on claim 4. Therefore, since claim 4, as amended, does not include the language that was the focus of the objection, claims 5 and 6 do not include the language that was the focus of the objection. Therefore, applicant requests withdrawal of the objections and reconsideration and allowance of claims 4-6.

The office action fails to provide a citation to an authority (statute, regulation, or MPEP section) for the objection to claim 14. Thus, applicant is unable to respond. Therefore, applicant respectfully requests that if the Examiner repeats the objection to claim 14 that the Examiner include a citation to a specific authority in the next office action, so the applicant can respond. If the Examiner cannot provide a citation to an authority for the objection, applicant requests withdrawal of the objection and reconsideration and allowance of claim 14.

Claim 15 is dependent on claim 14. For reasons analogous to those stated above, applicant requests withdrawal of the objection and reconsideration and allowance of claim 15.

§ 102 Rejections of the Claims

Claims 4, 14, and 15

Claims 4, 14, and 15 were rejected under 35 U.S.C. § 102(e) as being anticipated by Manning *et al.* (U.S. 5,962,887). Applicant does not admit that Manning *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. 1.131 to "swear behind" Manning *et al.* Applicant traverses the rejections of claims 14 and 15.

Claim 4, as amended, recites, "a gate oxide layer having a thickness of between about 20 angstroms and about 40 angstroms." In contrast, Manning *et al.* teaches only "a thin dielectric region" at column 1, line 59, so Manning *et al* fails to teach "a gate oxide layer having a thickness of between about 20 and about 40 angstroms." Hence, Manning *et al.* fails to teach each of the elements of claim 4. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 4. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 4.

Claim 14 recites, "a ground node located on the die" and "a power supply voltage node located on the die." In contrast, Manning *et al.* teaches at column 2, lines 7-10, ". . . NMOS capacitor 145 has a capacitance value which depends on the applied voltage, as described in . . . ." Thus, Manning *et al.* fails to teach "a ground node located on the die" or "a power supply voltage node located on the die." Hence, Manning *et al.* fails to teach each of the elements of claim 14. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 14. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 14.

Claim 15 is dependent on claim 14. For reasons analogous to those stated above, applicant respectfully submits that the office action fails to state a *prima facie* case of anticipation with respect to claim 15. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 15.

Claims 9 and 10

Claims 9 and 10 were rejected under 35 U.S.C. § 102(b) as being anticipated by Mead *et al.* (U.S. 5,844,265). Applicant respectfully traverses the rejection of claims 9 and 10.

Claim 9 recites, " a transistor coupled between the high power supply voltage node and the low power supply voltage node." In contrast, Mead *et al.*, in Fig. 1, teaches varactor structure 32 (column 3, line 23) connected between input line 18 (column 3, line 4) and output node 28 (column 3, line 17). Fig. 1 includes V_{dd} rail 20 (column 3, line 5) and ground rail 24 (column 3, line 12), but varactor structure 32 is not connected between these rails. Hence, Mead *et al.* fails to teach each of the elements of claim 9 arranged as recited in claim 9. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 9. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 9.

Claim 10 is dependent on claim 9. For reasons analogous to those state above, applicant respectfully submits that the office action fails to state a *prima facie* case of anticipation with respect to claim 10. Furthermore, applicant respectfully disagrees with the statement in the office action regarding claim 10. The office action states, "the gate is coupled to the high power supply voltage node and the source and drain are coupled to the low power supply voltage node." Clearly, for the varactor 32, shown in Fig. 1, the gate is connected to input line 18 (column 3, line 4) and the drain/source are connected to the output node 28 (column 3, line 17), so Fig. 1 does not teach, "the gate is coupled to the high power supply voltage node and the source and the drain are coupled to the low power supply voltage node," as recited in claim 10. Thus, the office action fails to state a *prima facie* case of anticipation with respect to claim 10. Therefore, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 10.

The office action, at page 6, states:

> In response to the arguments under the rejection anticipated by Mead *et al.*, it is clearly seen that the voltage at the gate (node 18) of Mead *et al.*'s transistor 32 is higher than the voltage at the drain and source (node 28) of transistor 32. Therefore, node 18 can be considered as high supply voltage node and node 28 can be considered as low supply voltage node of capacitor 32. The output voltage node (289) is determined by the value of capacitor 32. Therefore, capacitor 32 is operating to control the voltage at node 28.

Applicant respectfully submits that this analysis is incorrect. Thus, the rejections of claims 9 and 10 are not supported in the office action. Since the examiner is grounding the rejection of claims 9 and 10 on this analysis, applicant submits that the examiner is taking official notice of the operation of the circuit shown in Fig. 1 of Mead *et al.* Applicant respectfully objects to the taking of official notice of this incorrect analysis, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner provide an affidavit that includes the stated analysis. If the examiner cannot provide an affidavit, applicant requests withdrawal of the rejections and reconsideration and allowance of claim 9 and 10.

§ 103 Rejections of the Claims

Claims 5, 6, and 16

Claims 5, 6, and 16 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Manning *et al.* Applicant does not admit that Manning *et al.* is prior art and reserves the right, as provided for under 37 C.F.R. 1.131 to "swear behind" Manning *et al.* Applicant respectfully traverses the rejections of claims 5, 6, and 16.

Claim 5 recites, wherein the operating voltage value is between about .5 volts and about 1.5 volts. Claim 16 recites, " wherein the operational node voltage is about 1.3 volts.
The office action, paragraph 5, states, "the selection of the operation voltage to be between about 0.5 volts and bout [sic] 1.5 volts or at 1.3 volts is seen as a obvious design expedient dependent upon particular environment of use to ensure optimum performance." Applicant respectfully disagrees that the elements recited in claims 5 and 16 are an "obvious design expedient dependent upon particular environment of use to ensure optimum performance." Since applicant does not refer to "optimum performance" in the application and since all the elements of claim 5 and 16 are not found in the cited reference, applicant assumes that the Examiner is taking official notice of the missing elements from an undisclosed source. Applicant respectfully objects to the taking of official notice, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner cite a reference that teaches the missing elements. If the Examiner cannot cite a reference that teaches the missing elements,

applicant respectfully requests that the Examiner provide an affidavit that describes how the missing elements are present in the prior art. If the examiner cannot cite a reference or provide an affidavit, applicant requests withdrawal of the rejection and reconsideration and allowance of claims 5 and 16.

Claim 6 recites, "a logic cell coupled to the voltage node and located in close proximity to the transistor." The office action, at paragraph 5, states:

> However, it is seen as an obvious design choice for using the supply voltage (160) as a supply voltage for any logic cell and fabricate the logic cell close to the transistor dependent upon particular environment of use to ensure optimum performance.

Applicant respectfully disagrees that "a logic cell coupled to the voltage node and located in close proximity to the transistor" is an obvious design choice. Since all the elements of claim 6 are not found in the cited reference, applicant assumes that the Examiner is taking official notice of the missing elements from an undisclosed source. Applicant respectfully objects to the taking of official notice, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner cite a reference that teaches the missing elements. If the Examiner cannot cite a reference that teaches the missing elements, applicant respectfully requests that the Examiner provide an affidavit that describes how the missing elements are present in the prior art. If the examiner cannot cite a reference or provide an affidavit, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 6.

Furthermore, applicant also respectfully submits that an inconsistency exists between the office action and Manning *et al.* Manning *et al.* refers to reference number 160 as "a voltage 160" (column 2, line 12), while the office action refers to reference number 160 as "the supply voltage (160)." Applicant respectfully disagrees that "a voltage 160" is a supply voltage, and assumes that the Examiner is taking office notice that "the voltage 160" teaches or suggests "a supply voltage." Since all the elements of claim 6 are not found in the cited reference, applicant assumes that the Examiner is taking official notice of the missing elements from an undisclosed source. Applicant respectfully objects to the taking of official notice, and pursuant to M.P.E.P. § 2144.03, applicant traverses the assertion of official notice and requests that the Examiner cite

a reference that teaches the missing elements. If the Examiner cannot cite a reference that teaches the missing elements, applicant respectfully requests that the Examiner provide an affidavit that describes how the missing elements are present in the prior art. If the examiner cannot cite a reference or provide an affidavit, applicant requests withdrawal of the rejection and reconsideration and allowance of claim 6.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone applicant's attorney at 612-371-2109 to facilitate prosecution of the above referenced patent application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

RAJENDRAN NAIR ET AL.

By their Representatives,

SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A.
Attorneys for Intel Corporation
P.O. Box 2938
Minneapolis, Minnesota 55402
612-373-6900

Date July 11, 2003

By Danny Padys
Danny J. Padys
Reg. No. 35,635

CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Mail Stop AF, Commissioner of Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on this 11 day of July, 2003

KACIA LEE
Name

Kacia Lee
Signature